

FIG. 1 (Prior Art)

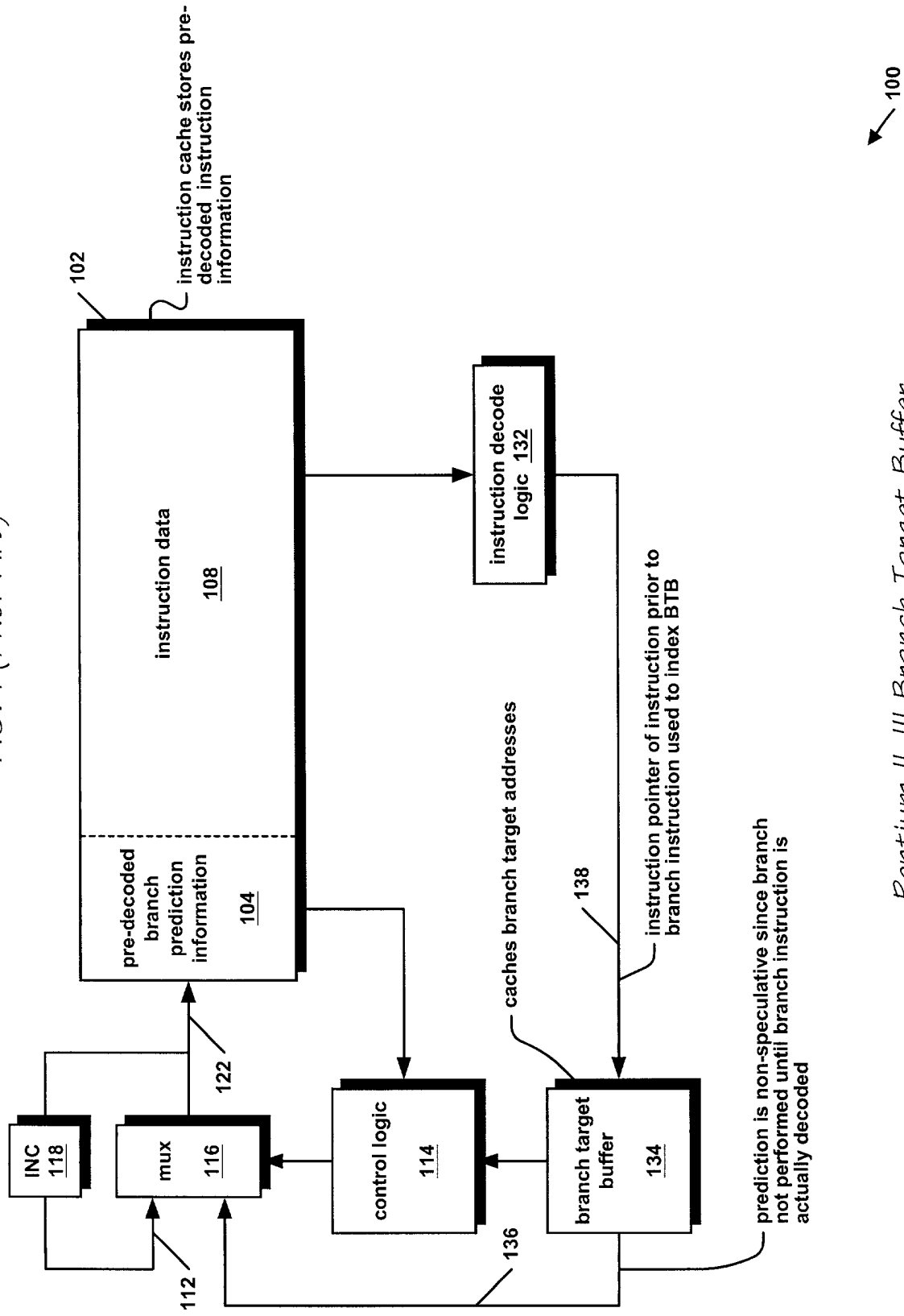
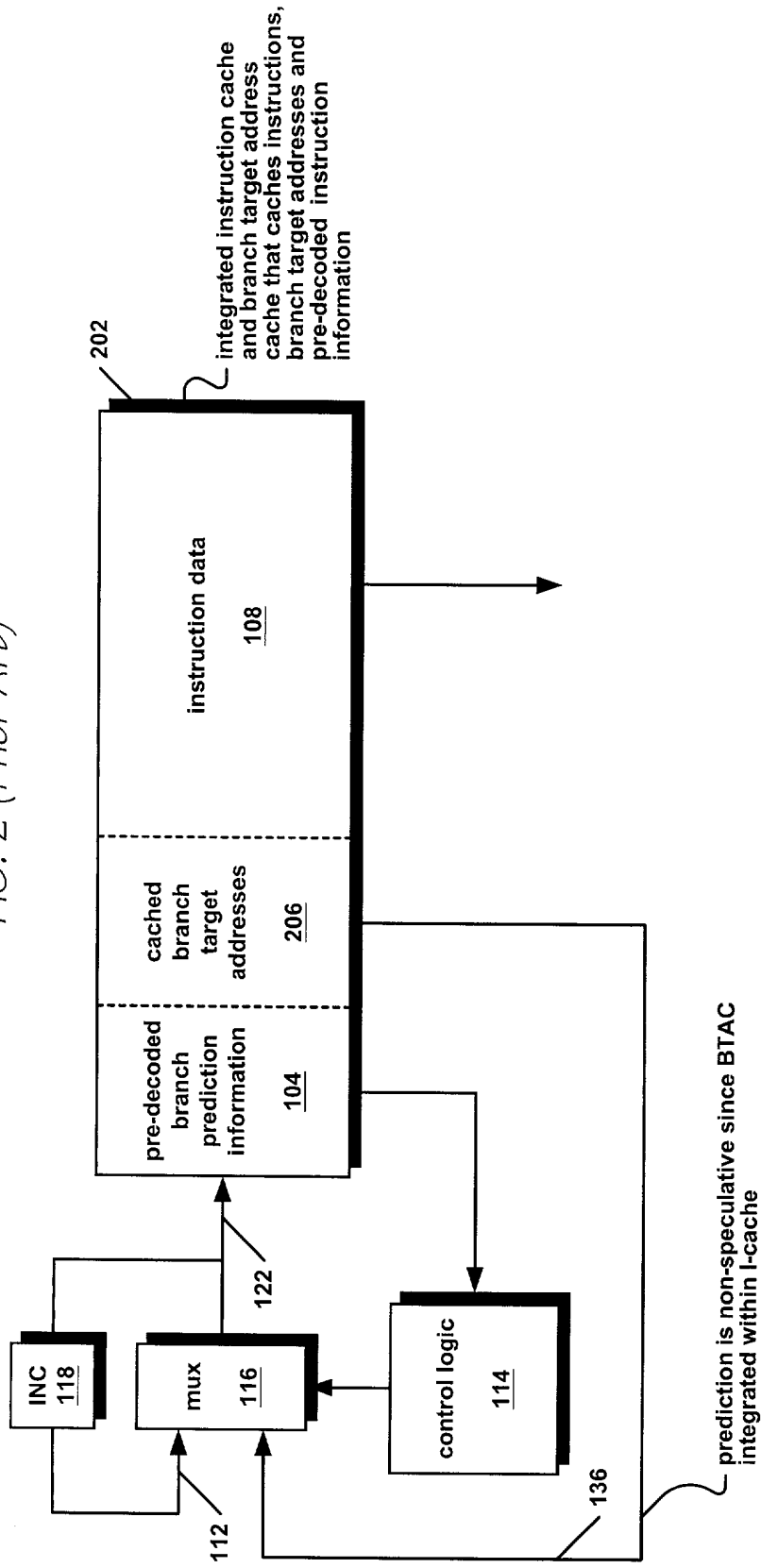
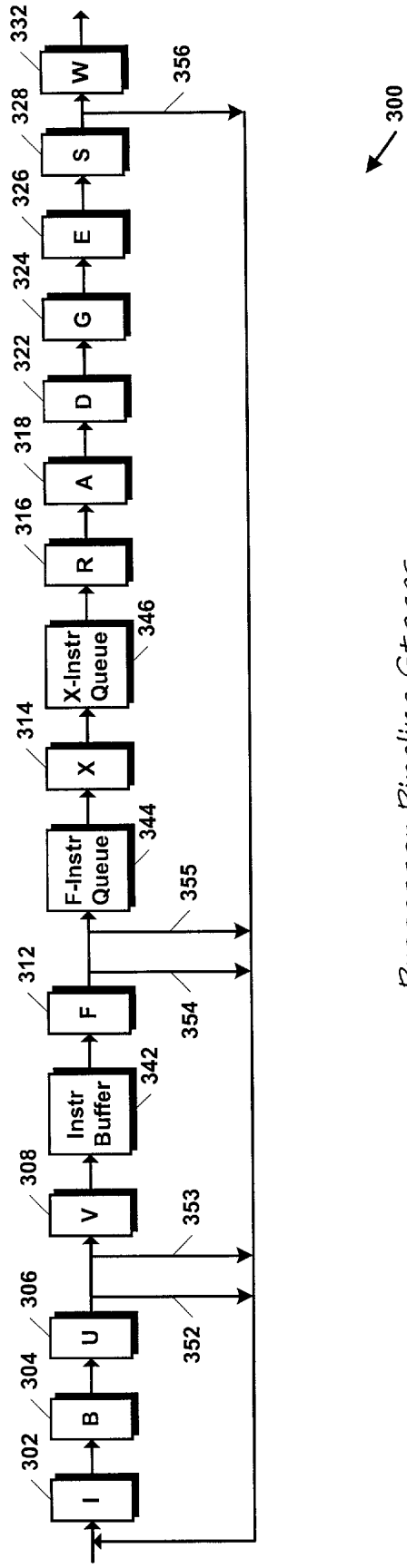


FIG. 2 (Prior Art)

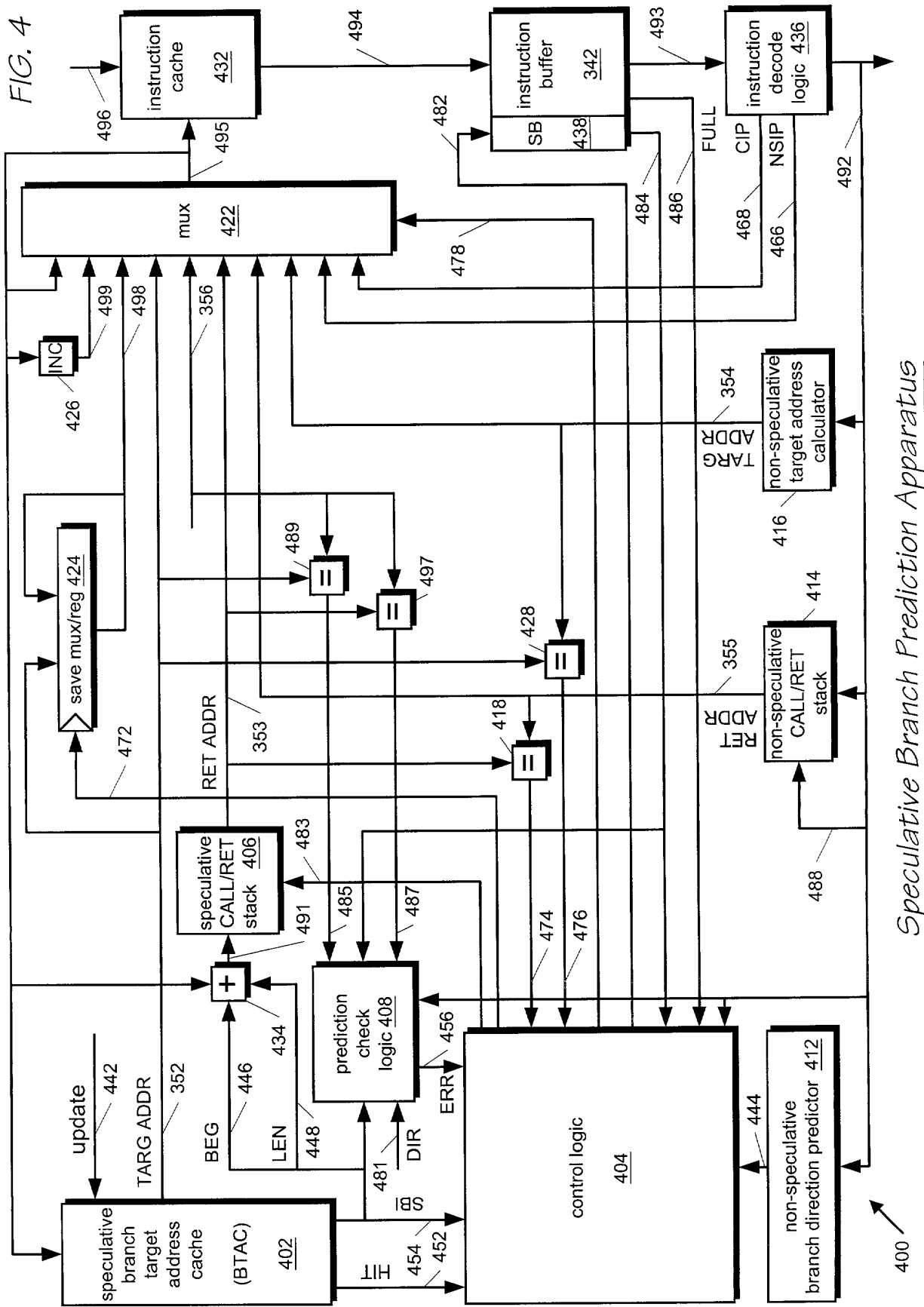


Athlon BTAC Integrated into Instruction Cache

FIG. 3

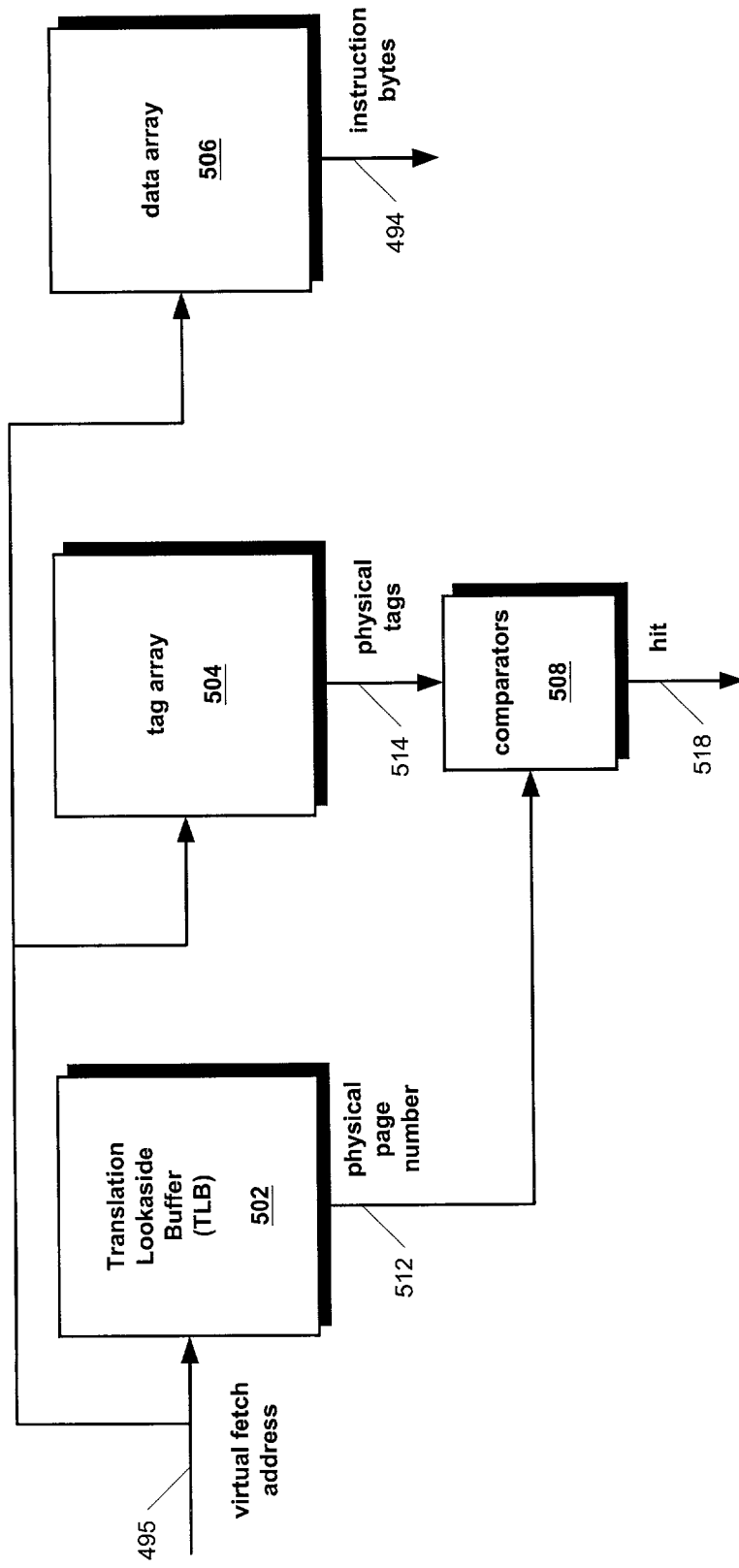


Processor Pipeline Stages



Speculative Branch Prediction Apparatus

FIG. 5



Instruction Cache

FIG. 6

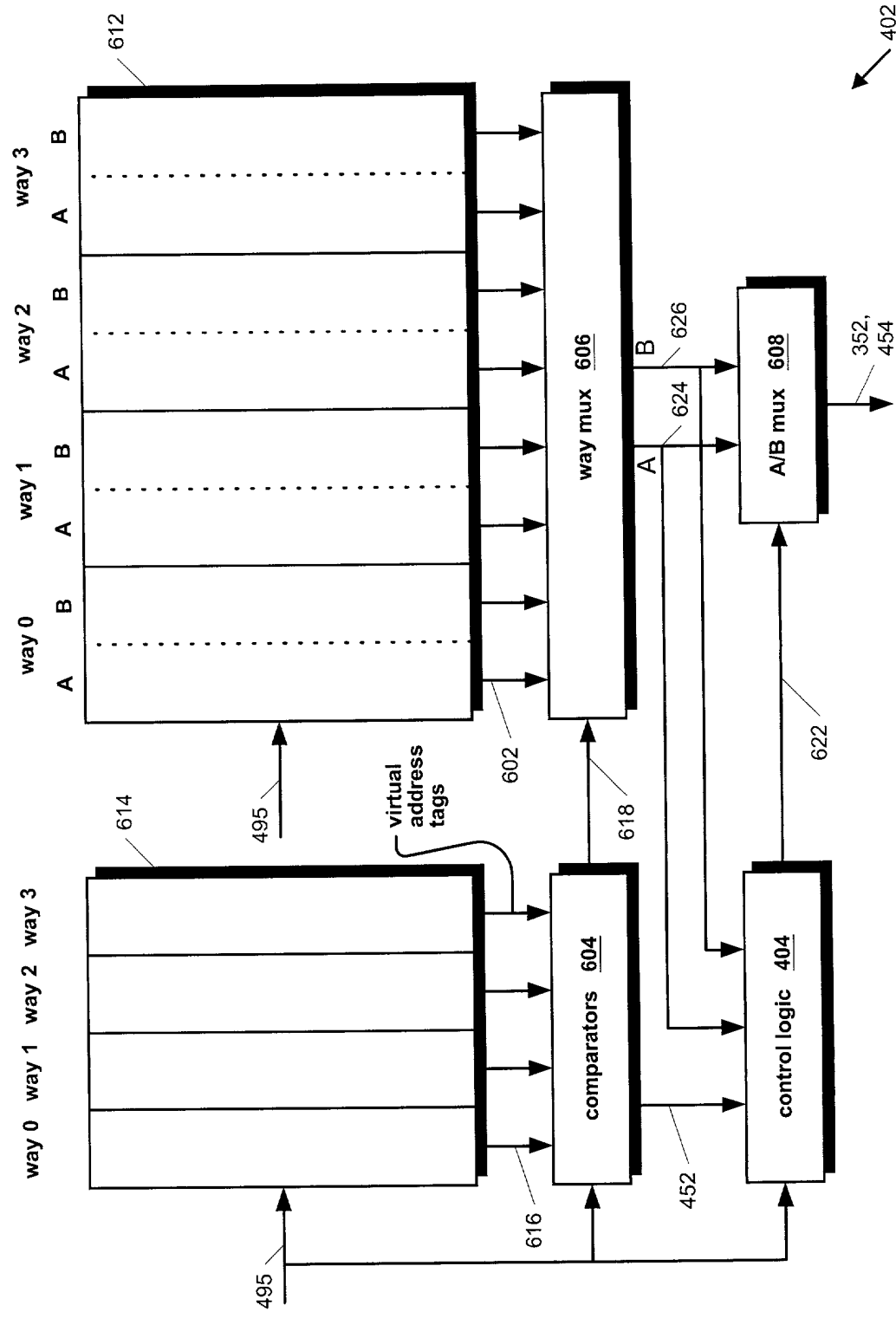
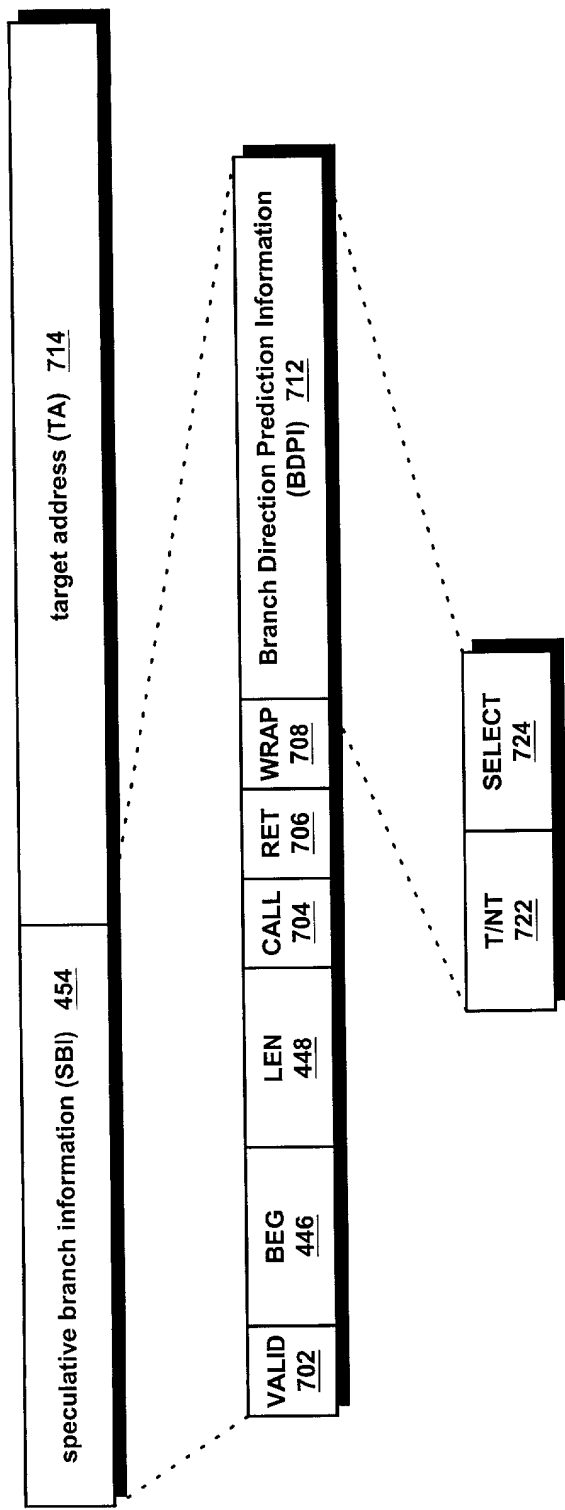
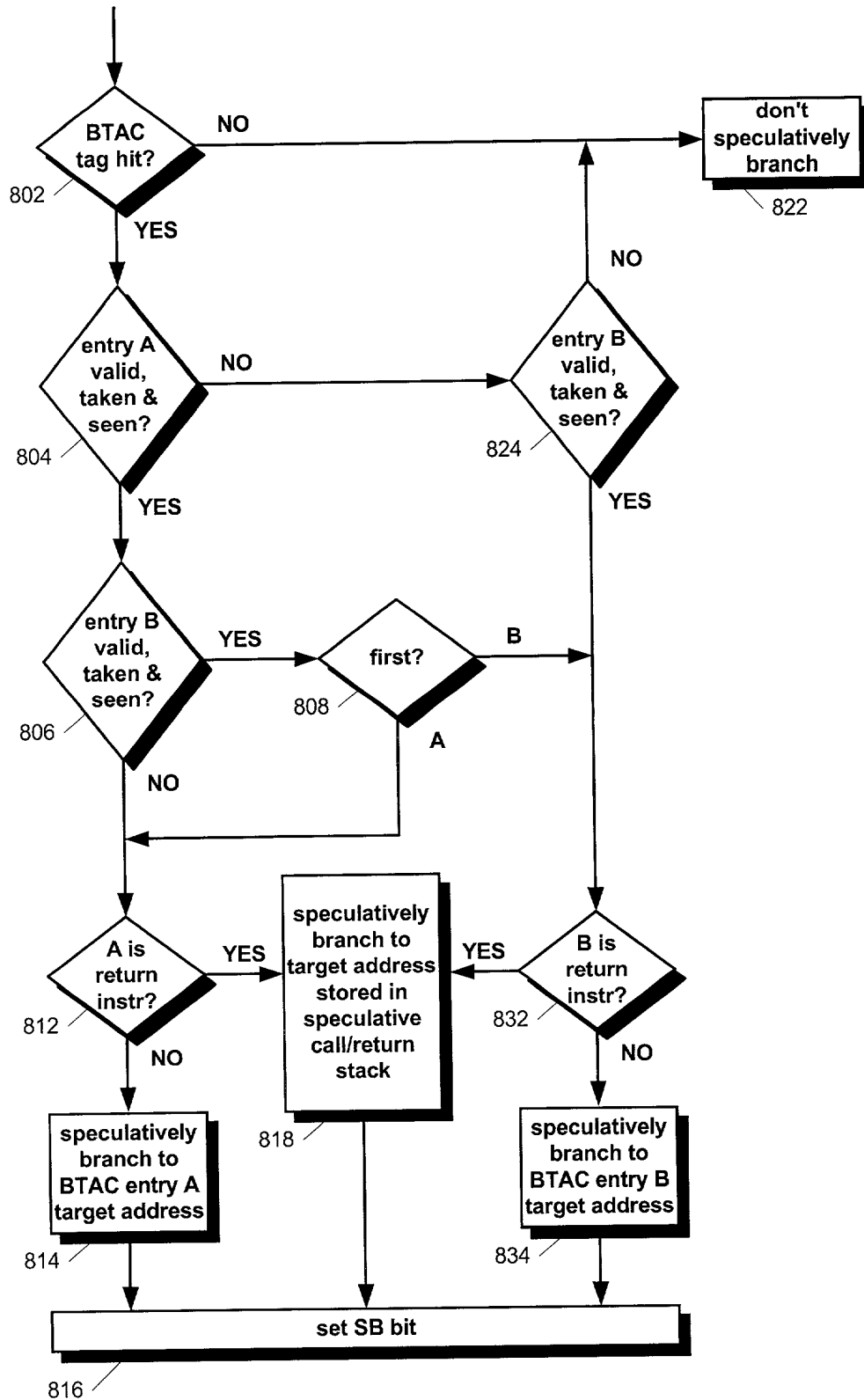


FIG. 7



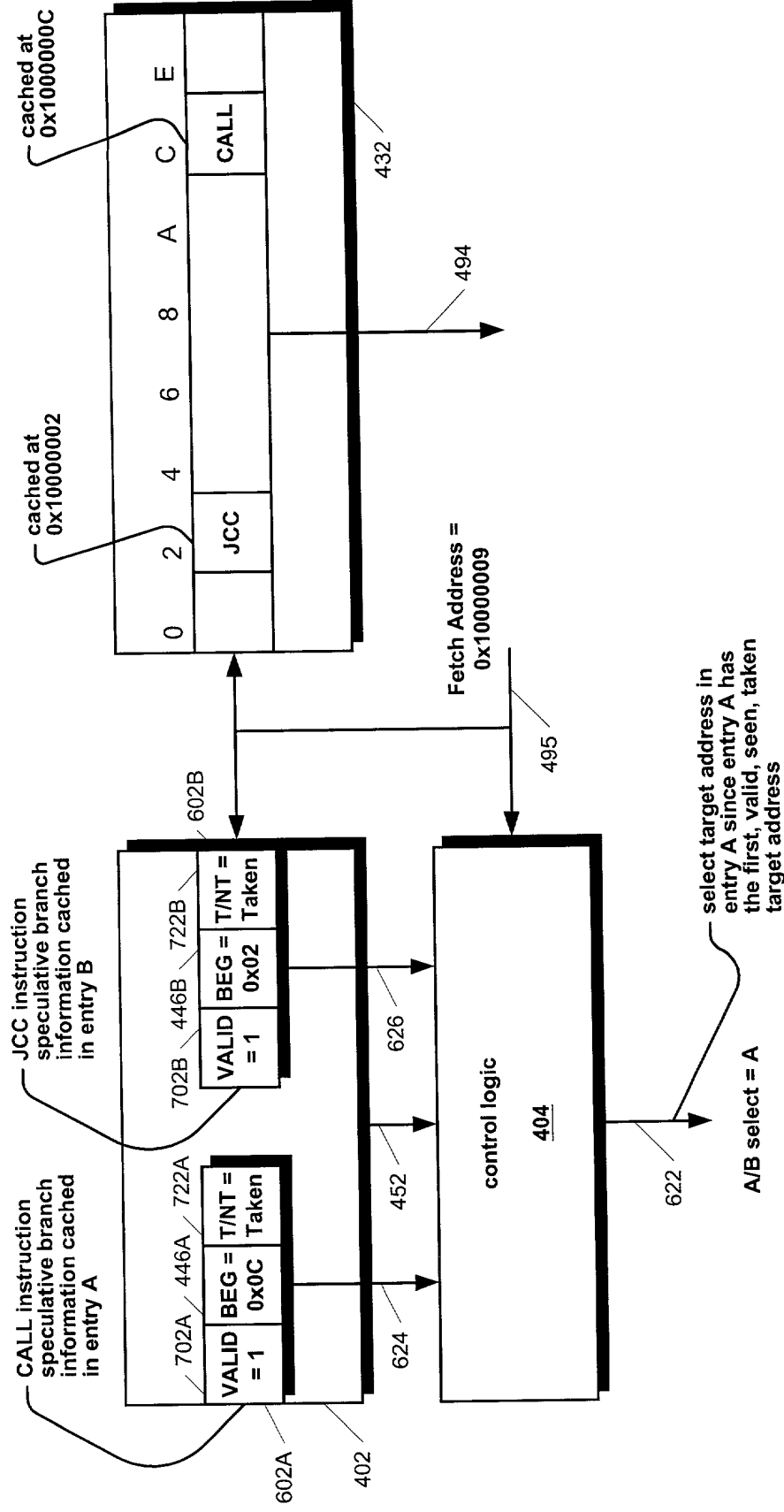
BTAC Entry

FIG. 8



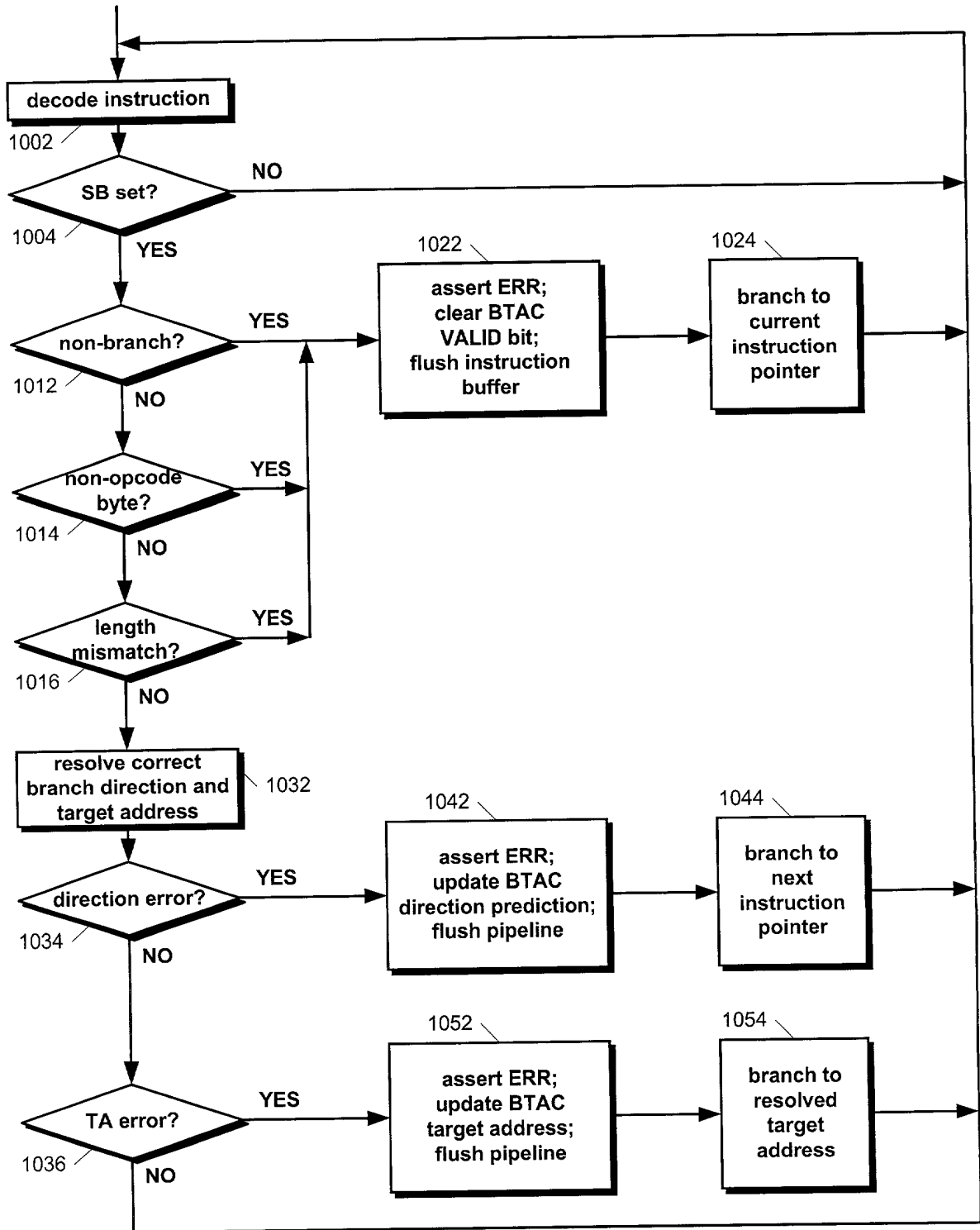
Speculative Branching Operation

FIG. 9



Target Address Selection Example

FIG. 10



Detection and Correction of
Speculative Branch Misprediction

FIG. 11

Previous Code Sequence:

0x00000010 JMP 0x00001234

...

Current Code Sequence:

0x00000010 ADD ;address 0x00000010 hits in BTAC generating a TA value of 0x00001234

...

0x00001234 SUB

0x00001236 INC

clock →	1	2	3	4	5	6	7
I-stage	ADD	X	X	SUB	INC	X	ADD
B-stage		ADD	X	X	SUB	X	X
U-stage			ADD	X	X	X	X
V-stage				ADD	X	X	X
F-stage					ADD	X	X

Cycle 1 = BTAC and I-cache access cycle

Cycle 4 = speculative branch cycle

Cycle 5 = speculative branch error detection cycle

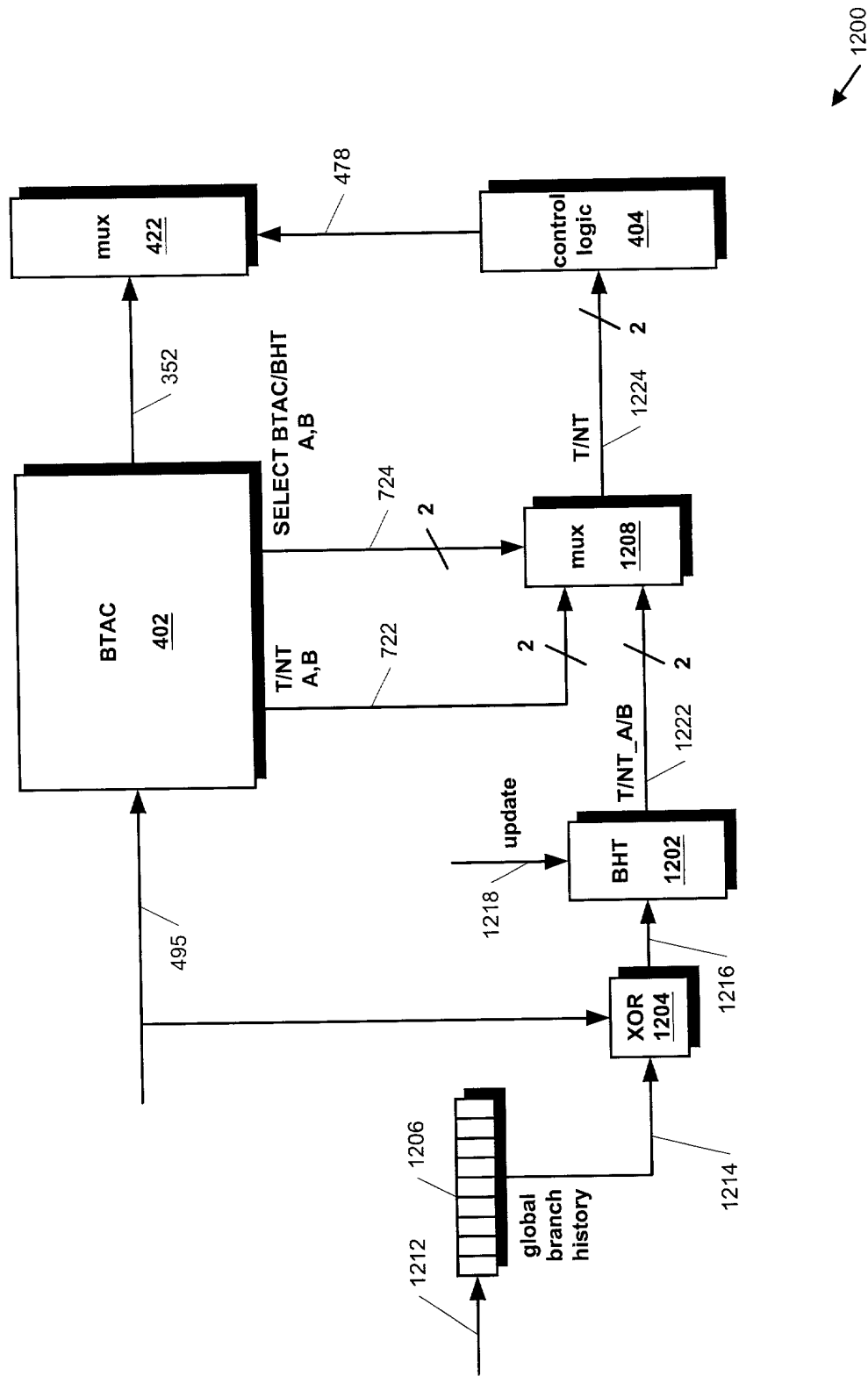
Cycle 6 = BTAC invalidate cycle

Cycle 7 = speculative branch error correction cycle

1100

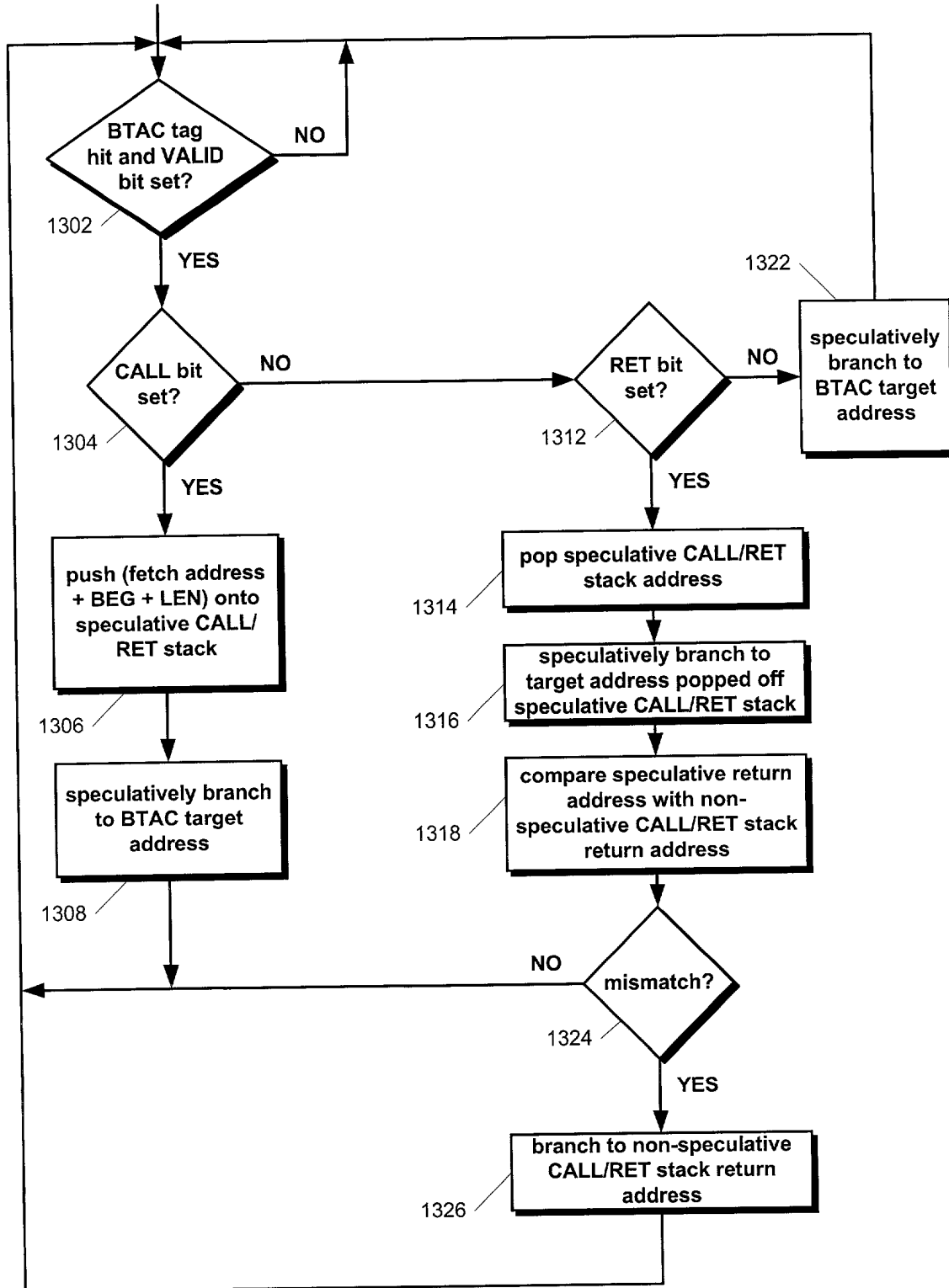
Misprediction Detection and Correction Example

FIG. 12



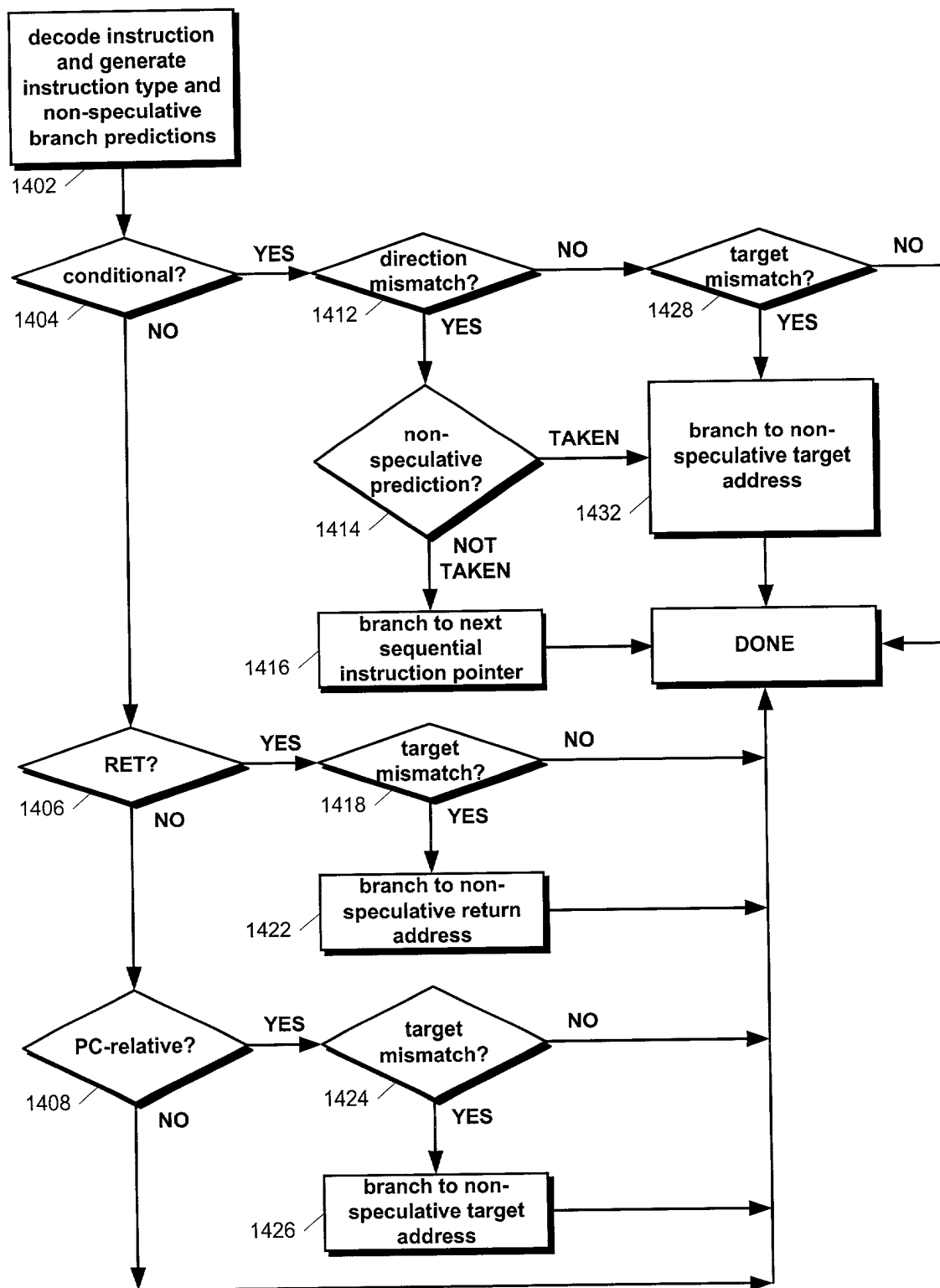
Hybrid Speculative Branch Direction Predictor

FIG. 13



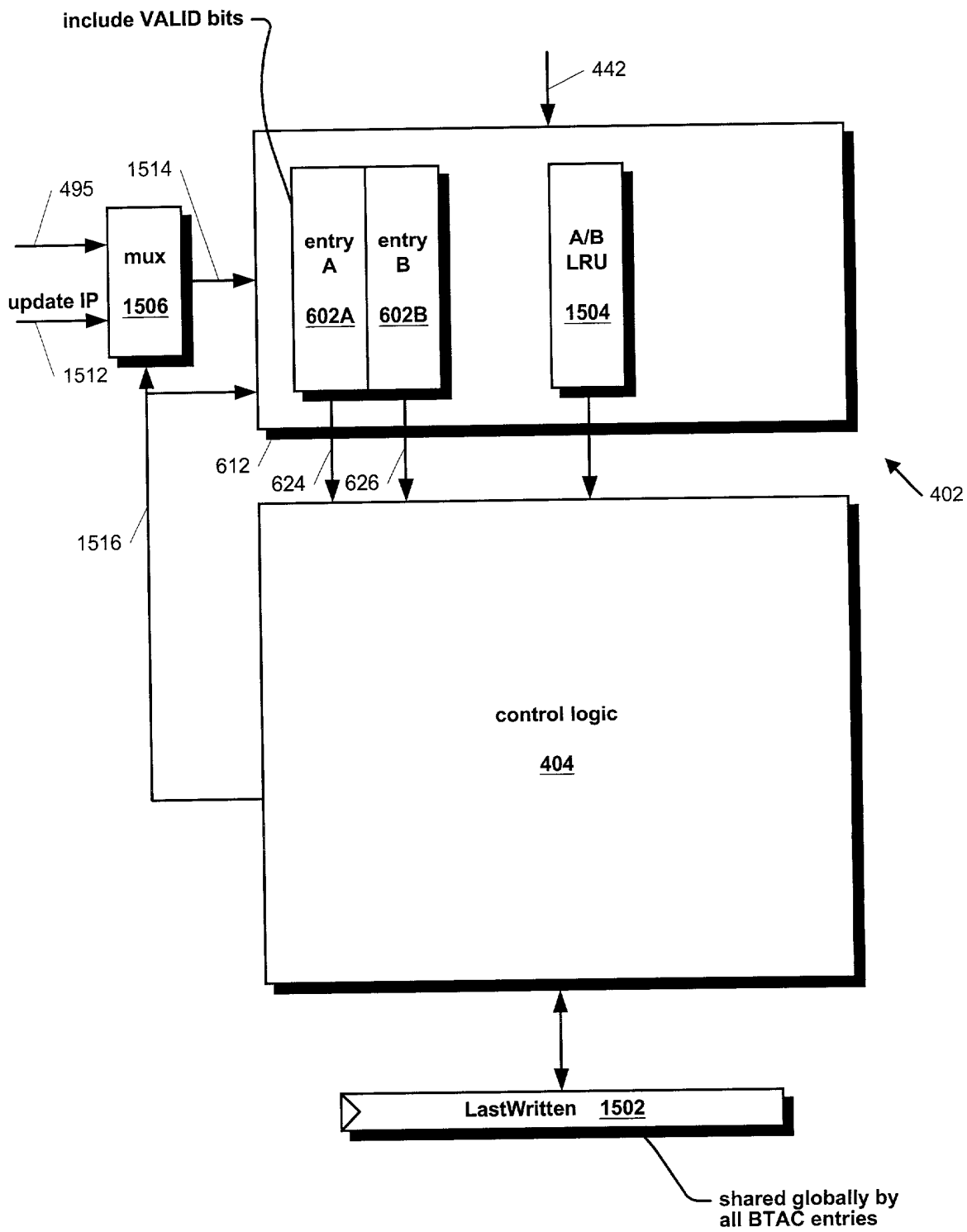
Dual CALL/RET Stack Operation

FIG. 14



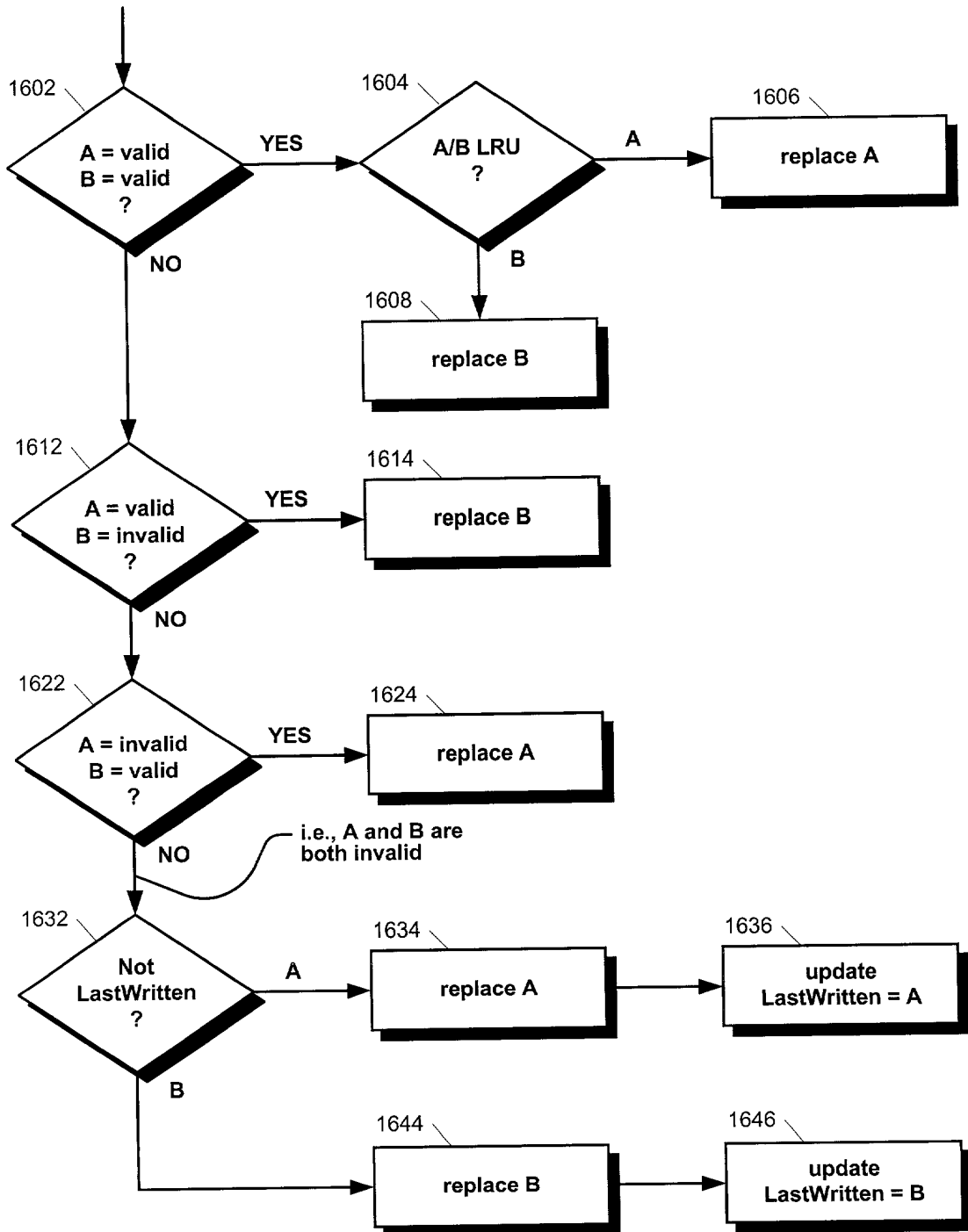
Selective Override of BTAC Prediction Operation

FIG. 15



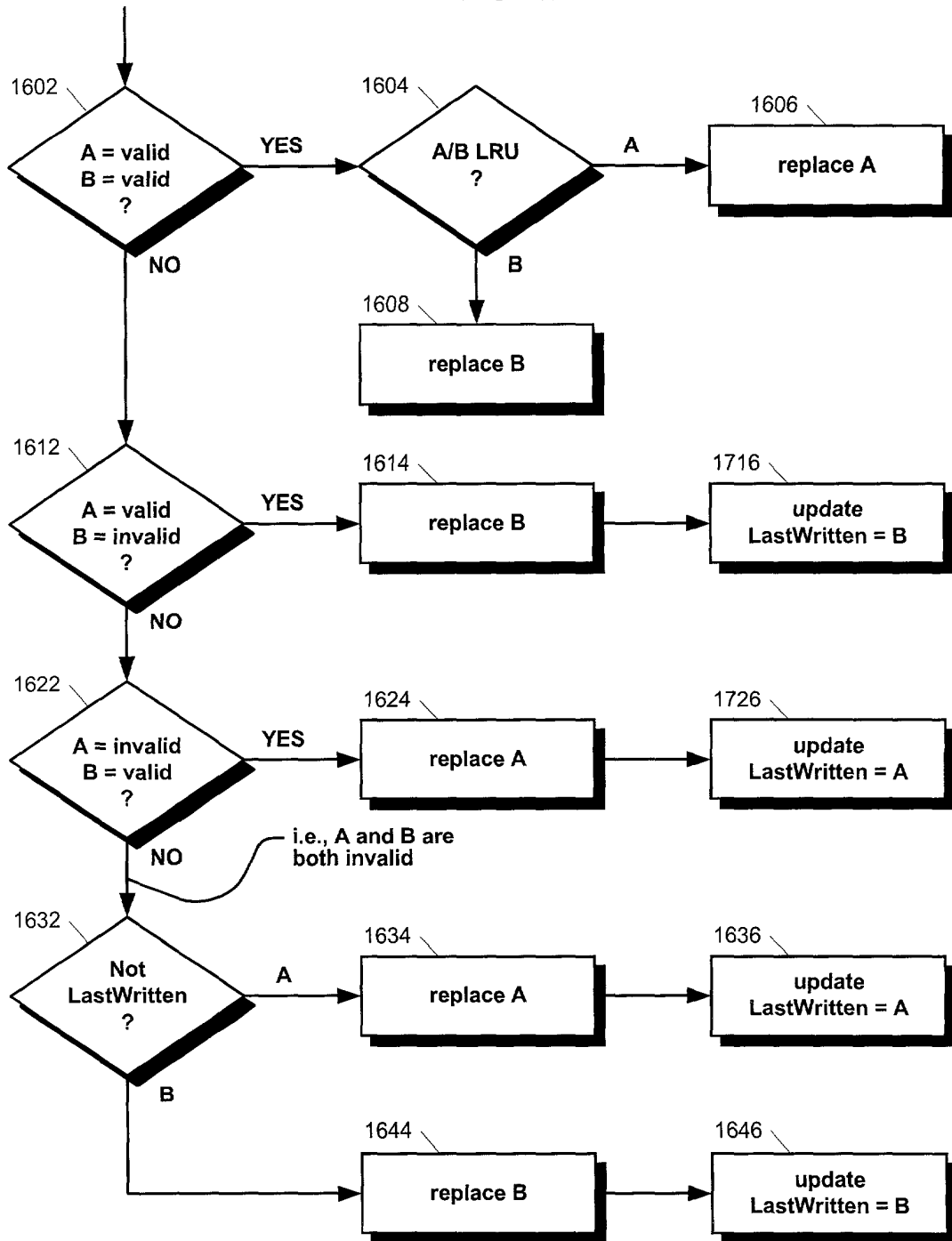
BTAC A/B Replacement Apparatus

FIG. 16



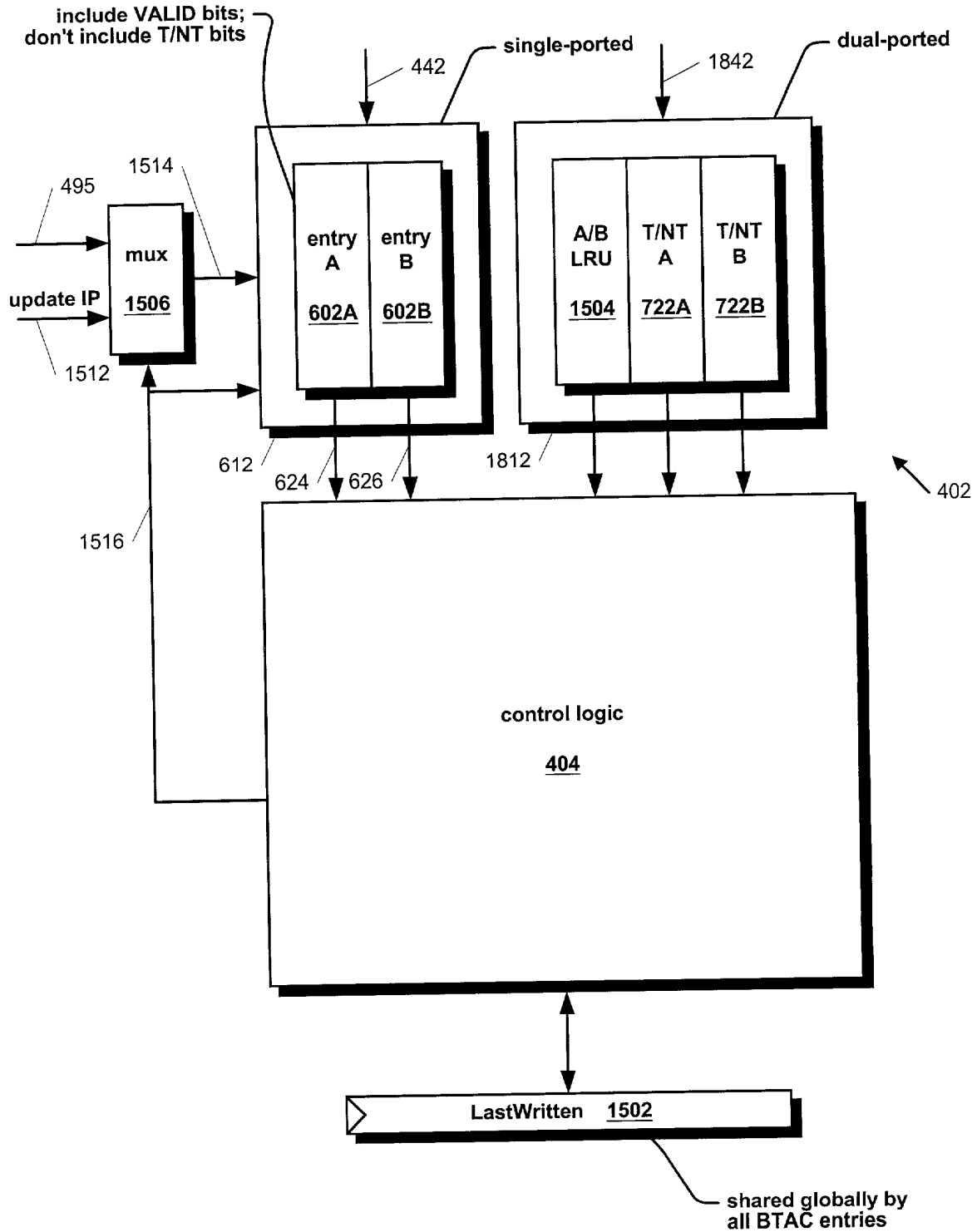
A/B Entry Replacement Method

FIG. 17



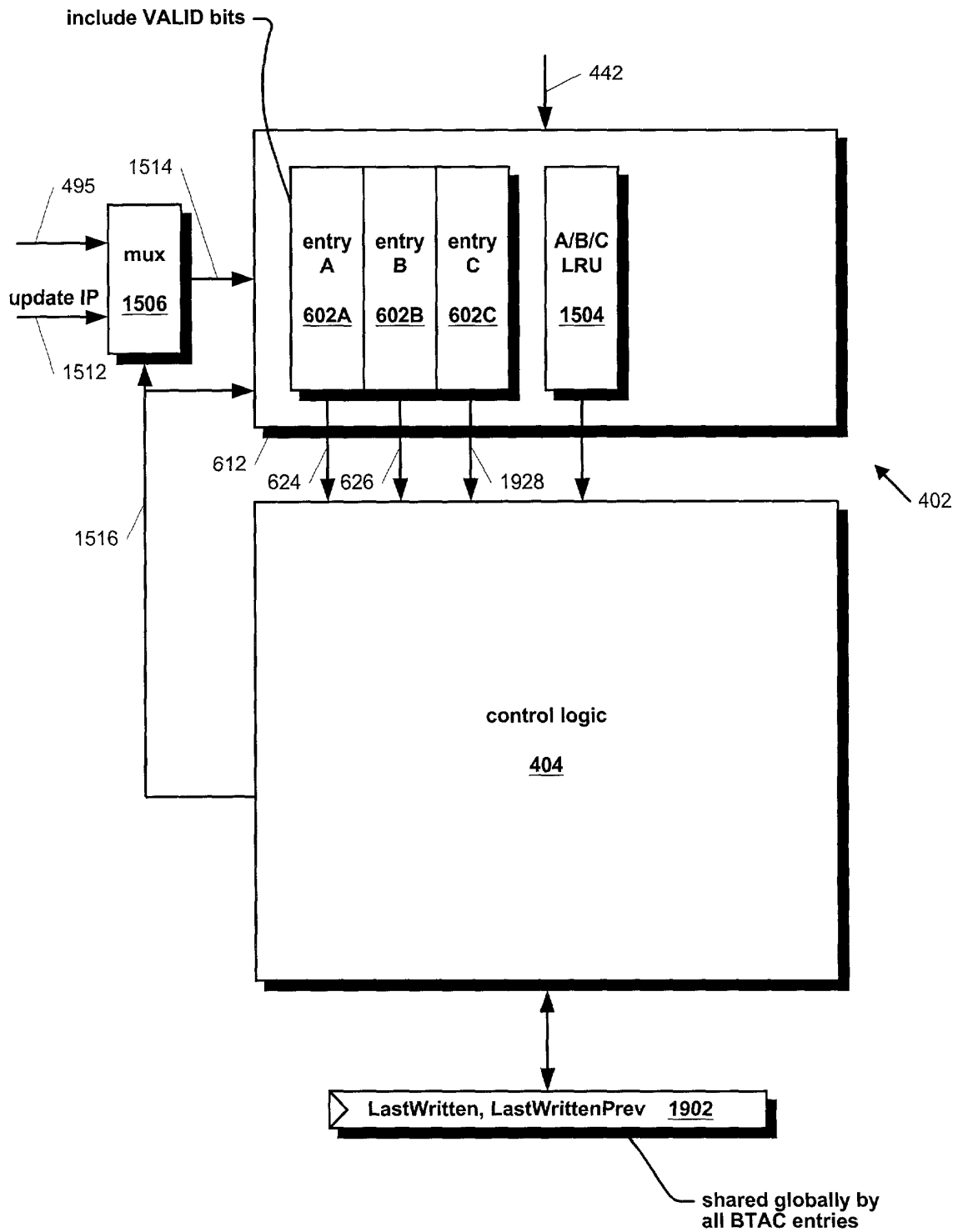
A/B Entry Replacement Method (Alt. Embodiment)

FIG. 18



BTAC A/B Replacement Apparatus (Alt. Embodiment)

FIG. 19



BTAC A/B/C Replacement Apparatus